Hardware Implementation of Two-Phase Bridgeless Interleaved Boost Converter for Power Factor Correction

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ABSTRACT
Conventional switched mode power supplies have high efficiency but low power factor which causes electromagnetic interface (EMI) problems. Designers improve power factor of these supplies with the help of power factor correction (PFC) circuitry. The function of the circuit is to force the converter to look like a resistive load to the line. In this paper, a single stage power factor correction using bridgeless Interleaved Boost Converter (IBC) has been proposed. The performance of the proposed converter is compared with the conventional boost, bridgeless boost and conventional IBC. Simulations of the circuit configuration of all three topologies are performed in MATLAB/SIMULINK. A comparative evaluation for all the topologies is presented in terms of supply current Total Harmonic Distortion (THD), Distortion Factor (DF) and supply Power Factor (PF). Hardware prototype of the proposed bridgeless IBC for power factor correction is developed to validate the results.
1. INTRODUCTION

DC power supplies are extensively used in many of the electrical and electronic appliances such as in computers, audio sets, televisions, and others. The presence of non-linear loads results in low power factor operation of the power system. The basic block in many power electronic converters are uncontrolled diode bridge rectifiers with capacitive filter. Due to the non-linear nature of bridge rectifiers, non-sinusoidal current is drawn from the utility and harmonics are injected into the utility lines. The bridge rectifiers contribute to high THD, low PF, and low efficiency to the power system. These harmonic currents cause several problems such as voltage distortion, heating, noises etc. which results in reduced efficiency of the power system. Due to this fact, there is a need for power supplies that draw current with low harmonic content and also have power factor close to unity. This results in the incorporation of power factor correction circuits. These circuits help to reduce the line current harmonics. Traditionally there are two ways of shaping the input current waveform so that the overall off-the-line AC-DC converter is seen as a resistive load by the ac mains. Firstly, by employing filters the power factor is improved: Passive Power Factor Correction (PPFC) and secondly by using proper DC-DC converters, the supply current is shaped: Active Power Factor Correction (APFC). PPFC increases the size of the system and therefore, currently, many researchers are working towards different topologies for APFC [1]. Active power factor correction involves reactive elements in conjunction with active switches, such as IGBTs, MOSFETs and thyristor which are switched at a desirable predetermined frequency [2-4]. These topologies result in source current shaping due to the fact that the active PFC topology always draws current in phase and at the same frequency as the line voltage. Thus, the power factor improves as the load becomes linear in nature. Following are some of the advantages of active PFC topologies:

- Controllable output voltage can be obtained
- Reduced harmonic distortion in line current
- Cheaper and less bulky components required
- Only part of the power is handled by the switching devices, resulting in higher efficiency

Based on the frequency of switching of the active devices involved, active power factor correction can be classified as: Low Frequency active power factor correction and High Frequency active power factor correction. In general, high frequency active power factor correction is preferred due to slow regulation of output voltage and the large size of reactive elements in low frequency active power factor correction topologies. In high frequency active power factor correction circuits, the load behaves like a resistor which brings the power factor closer to unity, thus minimizing the harmonics. Therefore, this paper focuses on the design and implementation of a two-phase bridgeless IBC for improving the power quality of the supply current waveform. The performance of the proposed converter is compared with various active PFC topologies namely the Buck Converter, Boost Converter and the Interleaved Boost Converter topologies [5-6]. Simulation studies are carried out in MATLAB/SIMULINK. A hardware model of the bridgeless IBC is implemented by employing MOSFET and the results are validated.

2. BRIDGELESS INTERLEAVED BOOST CONVERTER

This topology employs a bridgeless boost converter for active power factor correction. The prime feature of this topology is that the need for input diode bridge rectifier stage is eliminated completely, while still maintaining the classic boost topology [7-9]. The circuit diagram is shown in Fig.1. The Bridgeless Interleaved Boost Converter (IBC) topology for active power factor correction consists of a number of boost converters operating in parallel. The input diode bridge rectifier stage is eliminated while still maintaining the classic IBC structure. This topology affords a number of advantages in comparison to the conventional topologies. It addresses the heat management problem caused by the input diode rectifier stage of IBC. In effect, the bridgeless IBC topology combines the benefits of both the bridgeless topology and the interleaved structure. In the Bridgeless Interleaved Boost Converter topology, the rectifier stage is integrated with the high frequency converter. Due to the elimination of the bridge rectifier stage, the circuit becomes less bulky. Interleaving leads to an increase in the frequency of input current ripples and hence a reduction in the weight and volume of EMI filters required. The conduction losses are greatly reduced due to the presence of fewer number of semiconductor devices in each conduction path. In comparison to a two-phase IBC, a two-phase bridgeless IBC topology uses two extra MOSFETs and fast diodes, instead of the four slow diodes in the bridge rectifier stage. This converter topology thus affords the maximum efficiency due to the combined merits of interleaving and the bridgeless structure.
For analysis of the topology, the circuit is separated into two half cycles. Q1 and Q2 are turned on at the same instant and Q3 and Q4 are turned on at the same instant which is 180° out of phase with respect to the instants of Q1 and Q2. During the positive half cycle, Q1 and Q2 are turned ON and the current flows through L1, Q1, Q2 and L2 thereby storing energy in L1 and L2. When Q1 and Q2 are turned off, the energy stored in L1 and L2 are released as current through D1, load, body diode of Q2 and is fed back to the mains. Similarly, with a shift of 180°, Q3 and Q4 are turned ON and energy is stored in L3 and L4 via Q3 and Q4. During the negative half cycle, Q4 and Q2 are turned ON, energy gets stored in L2 and L1 for the first phase and L4 and L3 for the next phase and gets released as current which flows through D2 (D4), load, body diode of Q1 (Q3) and back to mains [10-12].

A new loss has been introduced in the intrinsic body diodes of the FETs, but since input bridge rectifiers are eliminated, there is some efficiency gain in overall performance of the topology. Overall, the MOSFETs are under more stress in bridgeless IBC topology, but the total loss for the proposed bridgeless interleaved boost are 40% lower than the benchmark conventional boost, 27% lower than the bridgeless boost and 32% lower than the interleaved boost. Since the bridge rectifier losses are so large, it is expected that bridgeless interleaved boost converter would have the least power losses in comparison to the other five topologies, discussed above [13-15]. It is to be noted that the losses in the input bridge rectifiers constitute 63% of total losses in conventional PFC converter and 71% of total losses in interleaved PFC converter. Therefore eliminating the input bridges in PFC converters is justified despite the fact that new losses are introduced.

3. SIMULATION RESULTS

The simulation circuit for the bridgeless interleaved boost converter is shown in Fig.2 and the design parameters are shown in Table: 1 for the proposed topology.
Table 1: Design parameters for the implementation of Bridgeless Interleaved Boost Converter Topology

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching Frequency</td>
<td>25kHz</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>20V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>40V</td>
</tr>
<tr>
<td>Duty Ratio</td>
<td>0.5</td>
</tr>
<tr>
<td>R1, R2, R3, R4</td>
<td>25milli ohms</td>
</tr>
<tr>
<td>L1, L2, L3, L4</td>
<td>667μH</td>
</tr>
<tr>
<td>C</td>
<td>975μF</td>
</tr>
<tr>
<td>R</td>
<td>47.06Ω</td>
</tr>
</tbody>
</table>

The simulation results for the supply voltage and supply current for bridgeless IBC is shown in Fig.3. The proposed topology is compared with Buck, Boost, Bridgeless boost and Interleaved boost rectifier is shown in Table 2.
Table 2: Comparative results of the performance parameters of the various Active Power Factor Correction Topologies

<table>
<thead>
<tr>
<th>Topology</th>
<th>THD (%)</th>
<th>Distortion Factor (kp)</th>
<th>Displacement Factor (kd)</th>
<th>Power factor (pf)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rectifier +Buck</td>
<td>147.93</td>
<td>0.5600</td>
<td>0.7180</td>
<td>0.4020</td>
</tr>
<tr>
<td>Rectifier +Boost</td>
<td>95.94</td>
<td>0.7220</td>
<td>0.8780</td>
<td>0.6330</td>
</tr>
<tr>
<td>Interleaved Boost</td>
<td>75.11</td>
<td>0.7990</td>
<td>0.9290</td>
<td>0.7420</td>
</tr>
<tr>
<td>Bridgeless Boost</td>
<td>69.12</td>
<td>0.8226</td>
<td>0.9995</td>
<td>0.8222</td>
</tr>
<tr>
<td>Bridgeless IBC</td>
<td>68.43</td>
<td>0.8252</td>
<td>0.9995</td>
<td>0.8248</td>
</tr>
</tbody>
</table>

From Table-2, it is found that the bridgeless IBC topology has the lowest value of Total Harmonic Distortion (THD) and the highest power factor of 0.9995. Hence this topology is chosen for implementation purpose.

4. HARDWARE IMPLEMENTATION

The following components are required to implement the Bridgeless Interleaved Boost Converter Topology for Active Power Factor Correction.

Table 3: Hardware Components for Bridgeless IBC

<table>
<thead>
<tr>
<th>Topology</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transformer</td>
<td>230V/15V, 1A</td>
</tr>
<tr>
<td></td>
<td>230V/24V, 1A</td>
</tr>
<tr>
<td>Bridge rectifier</td>
<td></td>
</tr>
<tr>
<td>Voltage regulator</td>
<td>15V</td>
</tr>
<tr>
<td>Power MOSFET</td>
<td>IRFP460A</td>
</tr>
<tr>
<td>Power Diode</td>
<td>1N5408</td>
</tr>
<tr>
<td>Smoothing capacitor</td>
<td>220uF</td>
</tr>
<tr>
<td>Optocoupler</td>
<td>MCT2E</td>
</tr>
</tbody>
</table>

4.1 Implementation of the Gating Circuit

The gating circuit basically involves the PIC18F4550 microcontroller which is programmed to generate the necessary switching pattern to trigger the MOSFETs of the power circuit.[16-19] As shown in Fig.4. The gating circuit is isolated from the power circuit using the MCT2E optocouplers. The 15 V DC supply to the optocoupler is obtained by feeding the 230 V AC supply to a network which comprises a transformer, diode bridge rectifier, filtering capacitor and a voltage regulator. The output of the
optocoupler is given across the gate and source terminals of the MOSFETs. The converter’s output can be seen across the Cathode Ray Oscilloscope (CRO). The schematic diagram is as shown below:

![Block Diagram](image)

**Fig.4 Block Diagram showing the implementation of the optocoupler circuit**

The PIC microcontroller generates the necessary switching pulses to be provided as input to the optocoupler IC 4N33 as shown in Figs.5, 6 & 7. The output of the optocoupler then triggers the Power MOSFETs. Two of the switches in the Bridgeless IBC topology are triggered at a frequency of 25 KHz (0.04 ms) while the other two switches are triggered at the same frequency, but with a phase lag of 180 degrees (i.e. a time lag of 0.02 ms). This switching pattern is generated at two output pins of the PIC microcontroller (pins 19 & 20- RD0 and RD1 respectively).

![Oscilloscope Image](image)

**Fig.5. Two 180 degree phase shifted square waves from the PIC inputs to the optocoupler**
The overall hardware for the bridgeless IBC is shown in Fig.8.
Fig. 9 shows for an input of 9V, the output voltage obtained is shown in PQ meter as 18.68V as the chosen duty ratio is 0.5.

Fig. 9 Multimeter showing the Input Voltage and Power Quality Analyzer showing the output voltage for the proposed IBC

Fig. 10 shows that the supply power factor obtained is about 0.713 which is close to simulation results.

6. CONCLUSION

This paper deals with a novel AC-DC converter topology, namely the Bridgeless IBC topology for active power factor correction. A comparative analysis of the performance parameters of the buck, boost, interleaved boost, bridgeless boost and bridgeless...
interleaved boost converter topologies for active power factor correction, has been carried out. The performance parameters obtained show that the bridgeless IBC topology affords the least total harmonic distortion and hence, the best power factor, which justifies its choice for final implementation purposes. The two phase Bridgeless IBC topology has thus been implemented in the open loop configuration. The experimental results obtained are found to closely match the simulation results.

REFERENCES

17. Datasheet of Optocoupler IC MCT2E.
18. Datasheet of Power MOSFET IRFP460A.