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PERFORMANCE ANALYSIS OF UNIFIED POWER FLOW CONTROLLER USING PROTEUS

ABSTRACT

The Unified Power Flow Controller (UPFC) was devised for the real-time control and dynamic compensation of ac transmission systems, providing multifunctional flexibility required to solve many of the problems facing the power delivery industry. Within the framework of traditional power transmission concepts, the UPFC is able to control, simultaneously or selectively, all the parameters affecting power flow in the transmission line (i.e., voltage, impedance, and phase angle). This paper provides the performance analysis of Unified Power Flow Controller (UPFC) under open loop and closed loop control for the power system applications.

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I INTRODUCTION

The ultimate reason that we are interested in power quality is the economic value. There are economic impacts on utilities, their customers, and suppliers of load equipment. The quality of power can have a direct economic impact on many industrial consumers. There has recently been a great emphasis on revitalizing industry with more automation and more modern equipment. This usually means electronically controlled, energy-efficient equipment that is often much more sensitive to deviations in the supply voltage than were its electromechanical predecessors. There is a big investment associated with these disturbances.

The electric utility is concerned about power quality issues. With today’s movement towards deregulation and competition between utilities, it is highly essential for the electric utilities to meet the customer expectations and customer confidence. Unified Power Flow Controller is one of the FACTS controllers that is used to for real time control and dynamic compensation of AC transmission systems. In order to address the power quality it is required to do performance analysis of the FACTS device deployed. This paper focuses on performance analysis of the Unified Power Flow Controller (UPFC) for AC transmission systems. In the proposed work, performance analysis is made for UPFC as it can independently control both the real power and reactive power in the transmission line.

This paper is organized as introduction in section I, the basic principle and operation of a UPFC connected to a network is presented in section II, open loop and closed loop control of UPFC is presented in section III, simulation results are presented in section IV, hardware setup is described in section V, conclusion is made in section VI, references in section VII and coding for programming PIC 16F87XA in provided in section VIII (appendix).

III OPEN LOOP AND CLOSED LOOP CONTROL OF UPFC

The block diagram of the proposed system illustrating the open-loop system for calculating UPFC shunt injected current is given in the fig.1 and the closed loop system for UPFC series injected voltage is given in fig.2

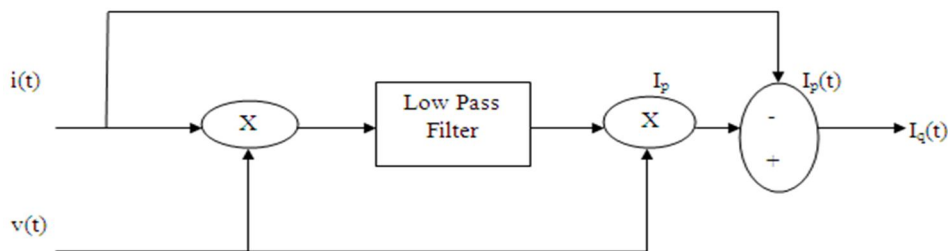


Fig.1 Open loop control of UPFC for calculating the shunt injected current

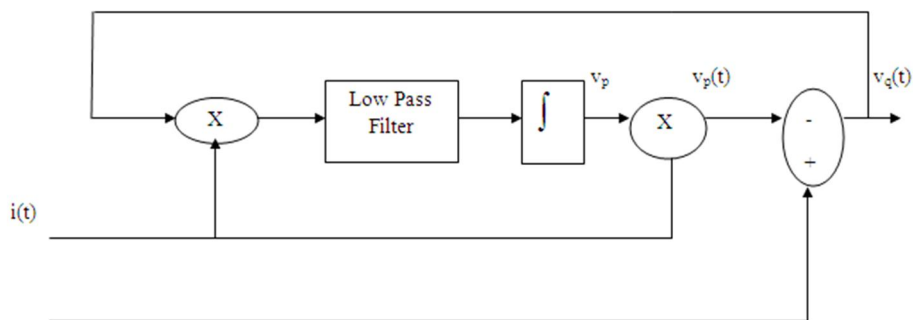


Fig.2 Closed loop control of UPFC for calculating the series injected voltage

The control algorithm is based on the active power filter reference current calculation method. Without UPFC shunt compensation, the line current, which is consisted of active and reactive components, is made up of the following terms: (neglecting the dc and harmonic components)

$$\begin{aligned}
 i(t) &= i_p(t) + i_q(t) \\
 &= I_p \sin(\omega t) + I_q \cos(\omega t) \quad (1)
 \end{aligned}$$

To regulate the voltage at bus connected to the shunt converter of the UPFC, the only component that this bus should supply is the active current component. Using eqn.(1), it can be noted that if the shunt converter of the UPFC supplies the reactive component, then the sending bus needs only to supply the active component. This can easily accomplished by subtracting the active current component from the measured line current

$$i_q(t) = i(t) - I_p \sin(\omega t) \tag{2}$$

In eqn. (2), I_p is the magnitude of the in-phase current (to be estimated) and $\sin(\omega t)$ is a sinusoidal in phase with the line voltage. From fig 1 we have,

$$i(t).\sin(\omega t) = \frac{I_p}{2} [1 - \cos(2\omega t)] + \frac{I_q}{2} [\sin(2\omega t)] \tag{3}$$

A series control algorithm is used for closed loop control of UPFC is shown in the fig.2.

IV. SIMULATION RESULTS USING PROTEUS

The block diagram of the proposed system is given in the figure below

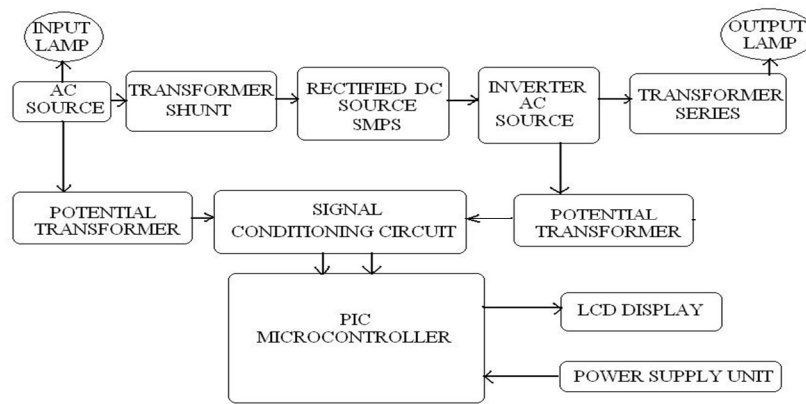


Fig.3. Block diagram of the proposed for performance analysis

Both the open loop and the closed loop control schemes are formulated in the proteus environment for performance analysis. The proposed system of UPFC (fig.3) is simulated using proteus software to analyze the performance of UPFC under open loop and closed loop.

The simulation model developed using proteus for performance analysis of UPFC is given in fig.4.

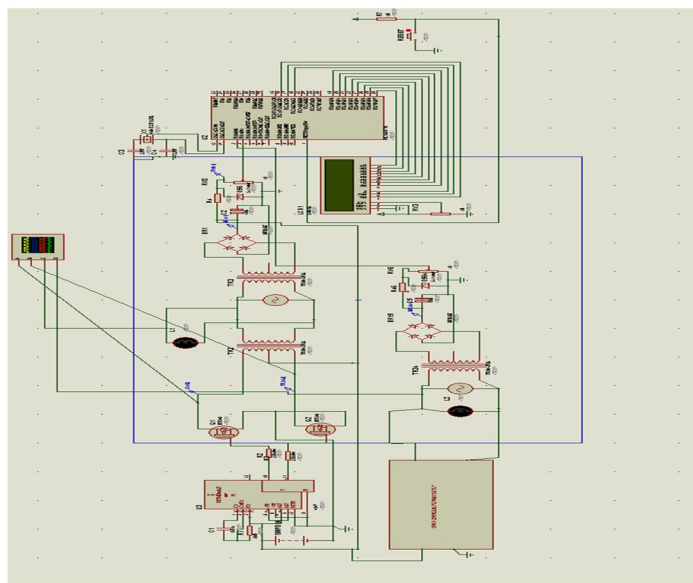


Fig .4.Simulation model developed using proteus for performance analysis of UPFC

The developed simulation model of UPFC using proteus software is simulated to analyze the open loop and the closed loop performance. The simulation results obtained are given in the fig.5.

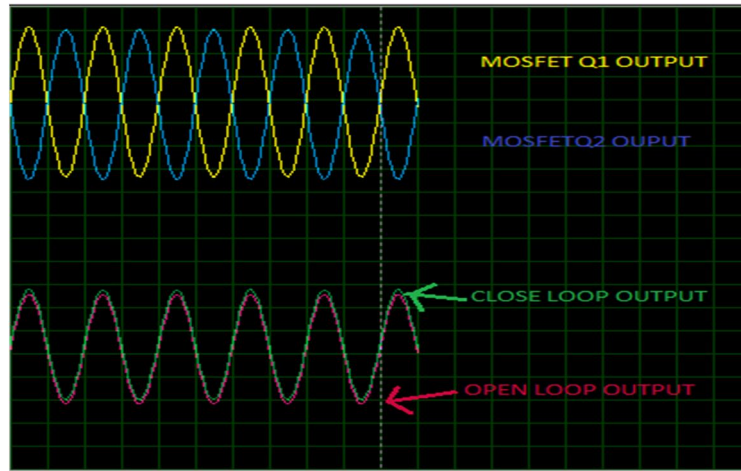


Fig.5. Simulation output of UPFC tested under open loop and closed loop conditions

From fig.5 we infer the yellow colored waveform represents the output of the MOSFET Q1 and the blue represents the output of the MOSFET Q2. The inverted output of the two MOSFET's is of pure sine waveform. The green colored waveform represents the output of the closed loop lamp whose magnitude is greater than magnitude of the open loop lamp and it is maintained constant during base load and peak loads operated on the same line. The pink colored waveform represents the output of the open loop lamp output whose magnitude oscillates due to load variations on the power line.

V .HARDWARE SETUP

In order to validate the simulation results a prototype model of the proposed system is created with the aid of the PIC microcontroller 16F87XA. The developed prototype model of UPFC to analyze the open loop and the closed loop performance is given in the fig.6.

The coding for the PIC microcontroller 16F87XA is done using MPLAB. The coding done for programming PIC 16F87XA is given in the appendix.

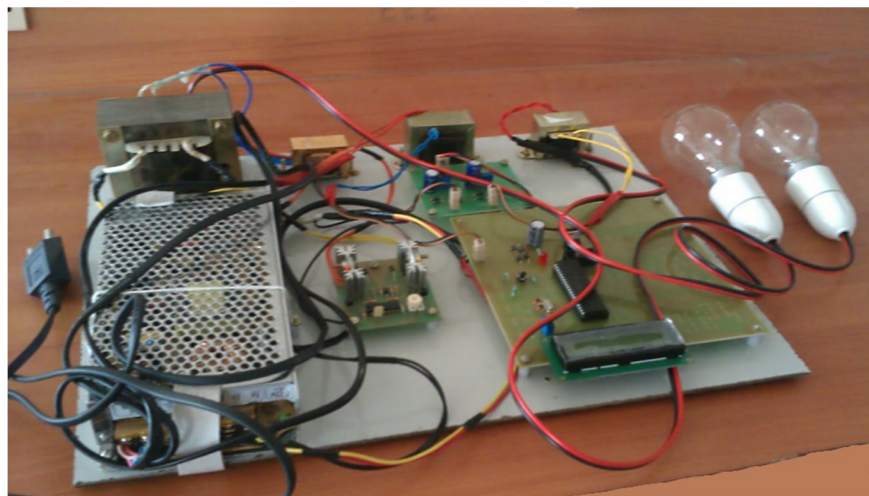


Fig.6 Developed prototype model of UPFC to analyze the open loop and closed loop performance

The prototype model is tested with various load conditions to make performance analysis. The results so obtained are given in table.1

S.No	Load	UPFC open loop control- line Voltage Magnitude with loads connected to the line	UPFC closed loop control- line Voltage Magnitude with loads connected to the line
1	100watts lamp(10)	100 V	232 V
2	Laptop charger	229 V	232 V
3	Fan	130 V	230 V
4	Iron box (750 watts)	98 V	230 V
5	Drilling machine(1000watts)	94 V	230 V

From table.1 we infer that with closed loop control of the UPFC the line voltage magnitude is maintained constant (i.e. 230 V) for almost all types of loads(100watts lamp, Laptop charger, Fan, Iron box (750 watts), Drilling machine(1000watts)) but in open loop control of UPFC the line voltage magnitude gets affected with the load variations. Under the open loop control of UPFC we observe that the load 2(laptop charger) alone line voltage magnitude is maintained as 230 V whereas for other loads (100watts lamp, Fan, Iron box (750 watts), Drilling machine (1000watts)) we could observe a great dip in line voltage magnitude (100 V, 130 V, 98 V, 94 V) which is not advisable. Hence with closed loop control of UPFC the line voltage magnitude can be maintained constant even for varying nature of loads. The experimental results obtained with the prototype model tested for varying load conditions comply with the simulation results obtained earlier thus validating the performance analysis stating the closed loop control of UPFC could yield better performance than the open loop control of UPFC.

VI SCOPE OF FUTURE WORK

The proposed method uses single UPFC with closed loop control to improve the power quality of the system by mitigating voltage sag, finally improving the stability at the customer utility. Scope of future work can be extended to more UPFC's with closed loop, connected in cascade manner in the power system to improve the stability of the system, improve voltage profile, controlled real and reactive power flow through the line, reduce the voltage sag and to improve the power quality at the customer utility.

VII REFERENCES

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VIII. APPENDIX

PIC MICROCONTROLLER CODING

```

#include<pic.h>
#include "lcd.h"
_CONFIG(XT & WDTDIS & PWRDIS & BORDIS & LVPDIS & WRTE & DEBUGDIS & DUNPROT & UNPROTECT);
unsigned int i=0,count,count1,T1,T2,T3,T4,vltg,crt,tmp,crt1,tmp1,vltg1;
unsigned char RX,VX,a1,a2,a3,a4,b1,b2,f,l,c1,c2,VHUDS,VTENS,VONES,CHUDS,CTENS,CONES;
void delay();
void main()
{
    ADCON1=0X82;
    TRISA=0xFF;
    TRISC=0X80;
    TRISD=0X00;
    TRISB=0XF0;
    PORTA=0;
    moveon=0;
    lcd_init();
    while(1)
    {
        ADCON0 = 0x81;                //ADC Ch = 0
        delay();
        ADGO=1;
        while(ADGO);                //status check
        tmp=ADRESH*256+ADRESL;
        crt=vltg =tmp/2;
        VHUDS=crt/100;
        crt=crt%100;
        VTENS=crt/10;
        crt=crt%10;
        VONES=crt;
        cursor_loc(0X80);
        display_string("INPUT=");
        display_data(VHUDS);
        display_data(VTENS);
        display_data(VONES);
        delay();
        ADCON0=0X89;
        delay();
        ADGO=1;
        while(ADGO);                //status check
        tmp1=ADRESH*256+ADRESL;
        crt1=vltg1 =tmp1/2;
        CHUDS=crt1/100;
        crt1=crt1%100;
        CTENS=crt1/10;
        crt1=crt1%10;
        CONES=crt;
    }
}

```

```
cursor_loc(0Xc0);
display_string("OUTPUT=");
display_data(CHUDS);
display_data(CTENS);
display_data(CONES);
        delay();
    }
}
void delay()
{
    for(i=0;i<=20000;i++);
}
```